IN THE CLAIMS:

The claims remain as follows:

1. (Previously Presented) A method of generating one or more voltages internally by a memory device, comprising:

obtaining temperature information indicative of the temperature of the memory device, wherein obtaining temperature information comprises reading one or more bits in a mode register; and

varying a level of one or more internally generated voltages based on the temperature information.

2. (Canceled) The method of claim 1, wherein obtaining temperature information comprises reading one or more bits in a mode register.

3. (Previously Presented) The method of claim 1, wherein a refresh rate of the memory device is also varied based on the one or more bits.

4. (Canceled) The method of claim 1, wherein obtaining temperature information comprises measuring the temperature of the memory device with an internal temperature sensor.

5. (Original) The method of claim 1, wherein varying the level of one or more internally generated voltages based on the temperature information comprises:

generating one or more control signals based on the temperature information; and

adjusting, based on the one or more control signals, at least one of an output voltage level of a detector or an output voltage level of a reference, wherein both the detector and the reference are part of a voltage generator.

6. (Original) The method of claim 5, comprising adjusting the output voltage level of both the detector and the reference.

7. (Original) The method of claim 5, wherein adjusting at least one of an output voltage level of a detector or an output voltage level of a reference comprises controlling one or more switches with the one or more control signals.

8. (Original) The method of claim 5, wherein adjusting at least one of an output voltage level of a detector or an output voltage level of a reference comprises modifying the output voltage of a voltage divider circuit by closing a switch shunting a resistor.

9. (Original) The method of claim 5, wherein each of the one or more control signals corresponds to a distinct temperature range and generating the one or more control signals comprises:

determining a distinct temperature range including the ambient temperature; and

setting the control signal corresponding to the distinct temperature range including the ambient temperature.

10. (Original) The method of claim 1, wherein at least one of the internally generated voltages is negative with respect to a ground reference.

11. (Original) A method of reducing subthreshold current in memory cells of a memory device, comprising:

generating, from a supply voltage, a boosted voltage greater than the supply voltage to be applied to a wordline of one or more of the memory cells during a memory cell access; and

varying the level of the boosted voltage based on temperature information indicative of a temperature of the memory device.

12. (Original) The method of claim 11, wherein varying the level of the boosted voltage based on temperature information comprises decreasing the level of the boosted voltage as device temperature increases.

13. (Original) The method of claim 11, wherein varying the level of the boosted voltage based on temperature information comprises adjusting the output level of at least one of a voltage detector and a voltage reference based on the temperature information.

14. (Original) The method of claim 13, wherein varying the level of the boosted voltage based on temperature information comprises increasing the output level of the voltage detector as device temperature increases.

15. (Original) The method of claim 13, wherein increasing the output level of the voltage detector comprises shunting a resistor of a voltage divider circuit.

16. (Original) The method of claim 11, wherein the temperature information is written to a mode register of the memory device by an external device.

17. (Original) The method of claim 16, wherein a refresh rate of the memory device is also varied based on the temperature information.

18. (Original) The method of claim 11, wherein the temperature information is generated by a temperature sensing component internal to the memory device.

19. (Original) The method of claim 11, further comprising generating a plurality of temperature control signals based on the temperature information, wherein each temperature control signal corresponds to a distinct temperature range.

20. (Original) The method of claim 19, wherein generating a plurality of temperature control signals comprises determining if a diode voltage is within one of the distinct temperature ranges.

21. (Previously Presented) A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

a mode register for supplying temperature information indicative of a temperature of the memory device; and

one or more voltage generators configured to vary a level of a generated output voltage supplied to at least one of the peripheral circuitry and the memory cells, based on the temperature information.

22. (Canceled) The method of claim 21, wherein the means for supplying temperature information comprises a mode register.

23. (Original) The method of claim 21, wherein the peripheral circuitry comprises refresh circuitry for refreshing the memory cells at a variable rate determined by the temperature information.

24. (Canceled) The memory device of claim 21, wherein the means for supplying temperature information comprises an internal temperature sensor.

25. (Original) A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

means for supplying temperature information indicative of a temperature of the memory device; and

a voltage generator configured to generate, from a supply voltage, a boosted voltage greater than the supply voltage and vary the level of the boosted voltage based on the temperature information.

26. (Original) The memory device of claim 25, wherein the boosted supply voltage is applied to a wordline of one or more of the memory cells during a memory cell access.

27. (Original) The memory device of claim 25, wherein the voltage generator is configured to decrease the level of the boosted voltage as the temperature of the memory device decreases, as indicated by the temperature information.

28. (Original) The memory device of claim 25, wherein the voltage generator varies the level of the boosted voltage in response to a plurality of temperature control signals generated based on the temperature information.

29. (Original) The memory device of claim 28, wherein:

distinct logic states of the control signals corresponds to distinct temperature ranges; and

the voltage generator is configured to adjust the boosted voltage to a different level for each distinct temperature range.

30. (Original) The memory device of claim 29, wherein:

the voltage generator comprises a voltage detector and a voltage reference; and

the voltage generator is configured to vary the level of the boosted voltage by varying an output voltage of at least one of the voltage detector and the voltage reference.